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Ltr	REVISIONS	DATE	INITIALS
A	AS ISSUED	8-15-79	JK M

Model No. | Stock No. 1MB5

Title TRANSLATOR CHIP

Description DETAILED SPECIFICATION | Date 8-15-79

By TOM KRAEMER | Sheet No. 1 of 15

Drawing No. A-1MB5-9212-1

TRANSLATOR CHIP DETAILED SPECIFICATION

I. General Description

1.1 The 1MB5 translator chip provides a interface between the 1LA8 or 1MB1 processor and an Intel 8049. It is designed to work with the 1MA8 buffer and 11 MHz 8049. The chip allows one byte of data to be transferred between the processors in a parallel fashion. An additional byte of control and status bits are available to both processors for handshaking. The chip provides for a psuedo-DMA mode to allow up to 26 kilobytes/second to be transferred between processors. External select code inputs allow several 1MB5 chips to be used in one system. A block diagram of the chip and a typical system application is given in Fig. 1.1 and 1.2.

1.2 Other documents applicable to this design include:
a.) Electrical specification
b.) Schematic diagram
c.) Flow chart

II. Functional Description

2.1 The 1MB5 contains two interfaces -- one to the 1LA8/1MB1 and the other to the Intel 8049 -- and several control sections. These are described in detail below.

2.2 All communication between processors is done via the 1MB5's four registers.

Register	1LA8/1MB1 can	8049 can
Output Buffer (OB)	write only	read only
Input Buffer (IB)	read only	write only
Calculator Control (CCR)	write only	read only
Processor Status (PSR)	read only	write only

Data is transferred through the input and output buffers. Control and status bits for handshaking are put in the calculator control register and the processor status register. Notice that all registers are read only for one processor and write only for the other processor.

2.3 When the CCR or PSR are read the least significant bit indicates that the input buffer is full (IBF) -- a byte has been written to the input buffer but has not been read. The most significant bit indicates that the output buffer is full(OBF)-- a byte has been written to the output buffer but has not been read. In normal operation the processor uses these bits to tell it when it can read and write a byte of data. OBF and IBF are automatically set and reset when a write or read occurs.

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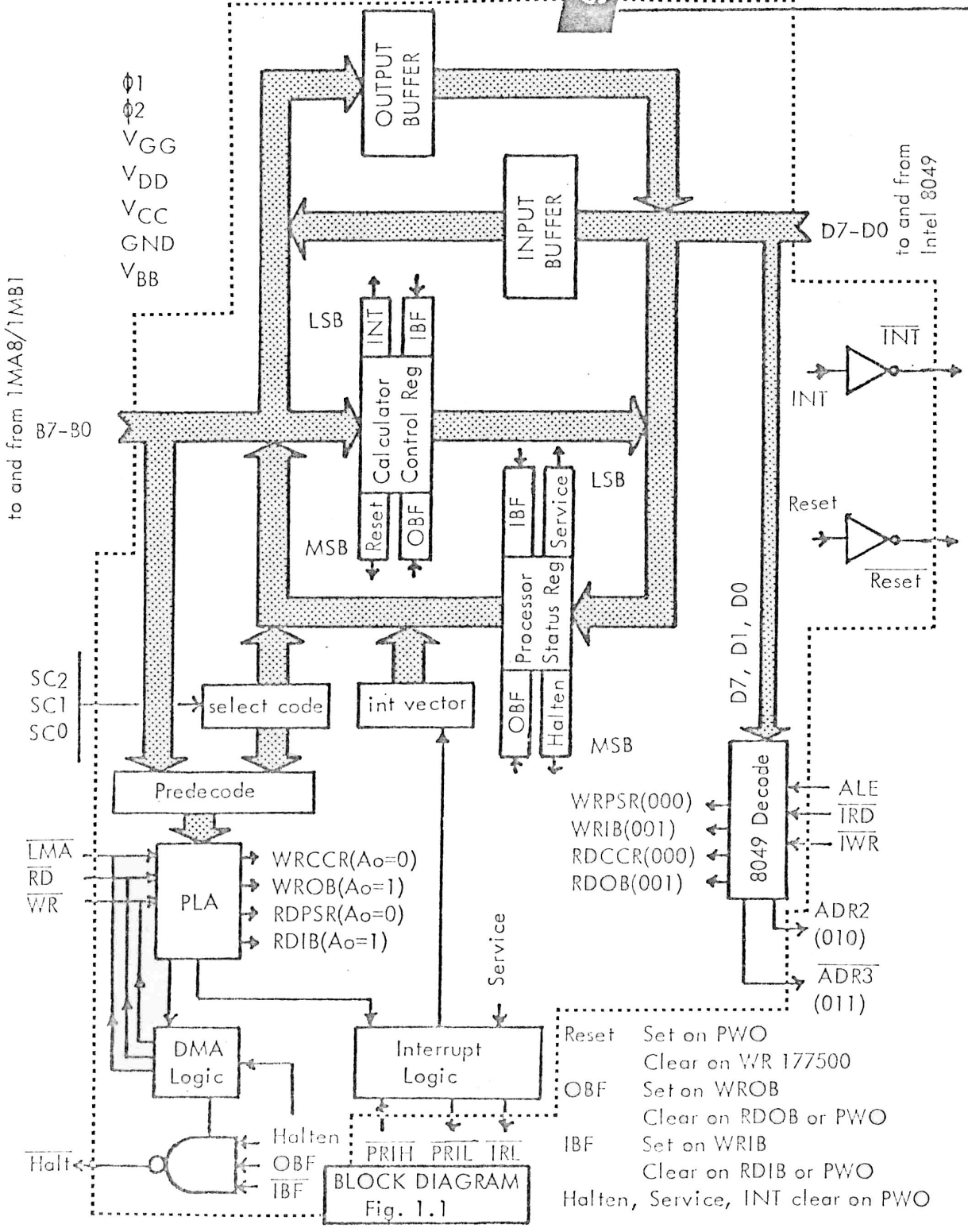
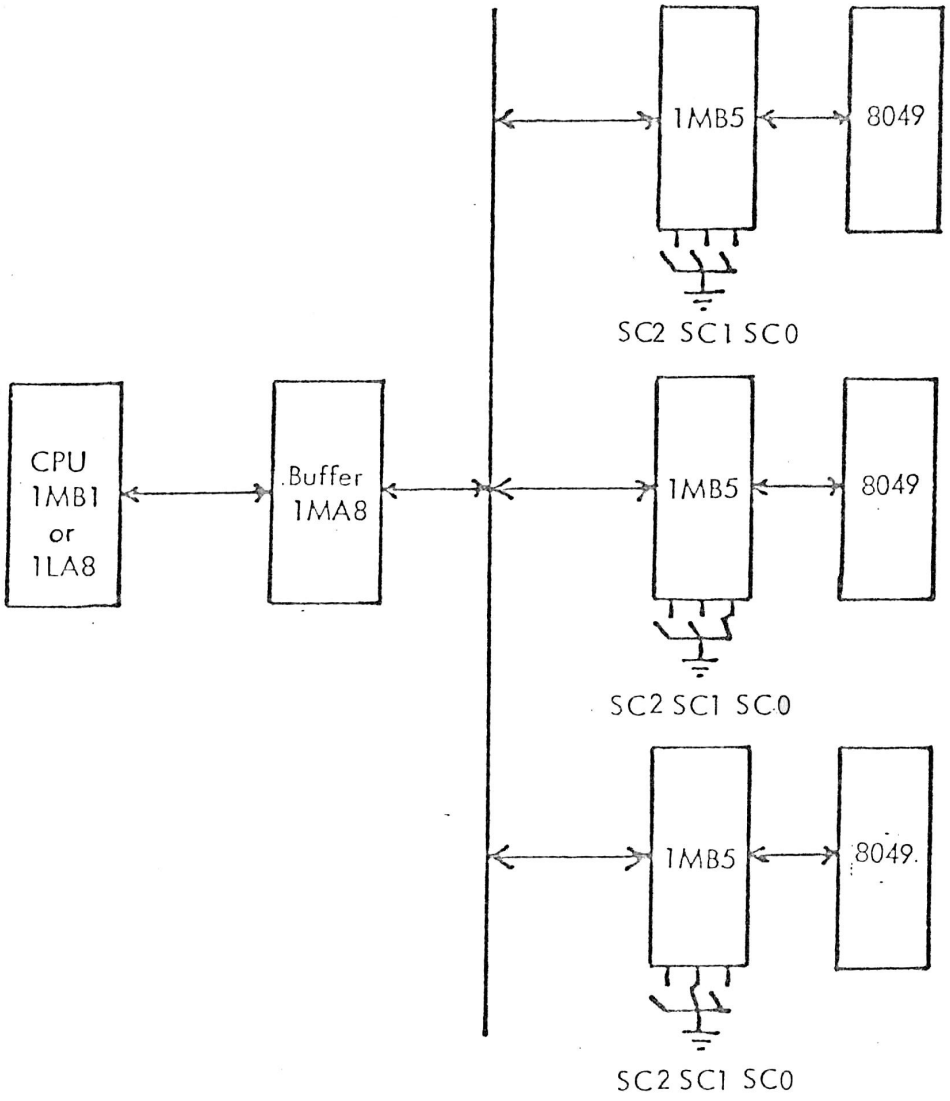


BLOCK DIAGRAM
Fig. 1.1

	SEE	SHEET 1		MODEL	STK NO.
				DETAILED SPECIFICATION - TRANSLATOR CHIP	
				BY TOM KRAEMER	DATE 8-15-79
				APPD	SHEET NO 3 OF 15
LTR	E.C. NO	APPROVED	DATE		



TYPICAL SYSTEM APPLICATION
Fig. 1.2

2.4 Each processor can interrupt the other processor. The 8049 can be and at power on is hardware reset by the 1LA8/1MB1 processor via the translator chip. The 8049 can cause the 1LA8/1MB1 processor to halt if the output buffer is full and the input buffer is empty and the bit Halten =1.

2.5 When three external switches are added to the 1MB5 select code input up to eight 1MB5's can be addressed by the 1LA8/1MB1. A metal mask or bonding option is available to provide for seven additional 1MB5's. The select code inputs have on chip pull-ups and thus they may be left open or grounded. Each 1MB5 must have a unique setting of the select code switches.

2.6 Multi-level interrupt capability is provided by the 1MB5. After each interrupt the 1LA8/1MB1 can read the select code of the 1MB5 which generated the interrupt.

III. Interface Description

3.1 Fig. 3.1 shows the pin assignments of the 1MB5 and a detailed description of each pin is listed in Table 3.1.

3.2 The 1MB5 responds as follows to these 1LA8/1MB1 I/O addresses.

Address(octal)	Control	Function
177400	WR	Global interrupt enable
177401	WR	Global interrupt disable
177500 or 177501	WR	Enables all 1MB5's interrupts. Drives 8049 $\overline{\text{RESET}}$ pin high.
	RD	Reads select code of the 1MB5 which interrupted. This location can be read only once after each interrupt. The select code is read in the following format:

BIT	MSB7	6	5	4	3	2	1	0 LSB
	0	1	0	SC3	SC2	SC1	SC0	0

where SC3=1 if not bonded see fig. 3.3

The 1MB5 also responds to these two addresses from the 1LA8/1MB1.

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB	Read	Write
1	1	1	1	1	1	1	1	0	1	0	SC3	SC2	SC1	SC0	0	PSR	CCR
1	1	1	1	1	1	1	1	0	1	0	SC3	SC2	SC1	SC0	1	IB*	OB**

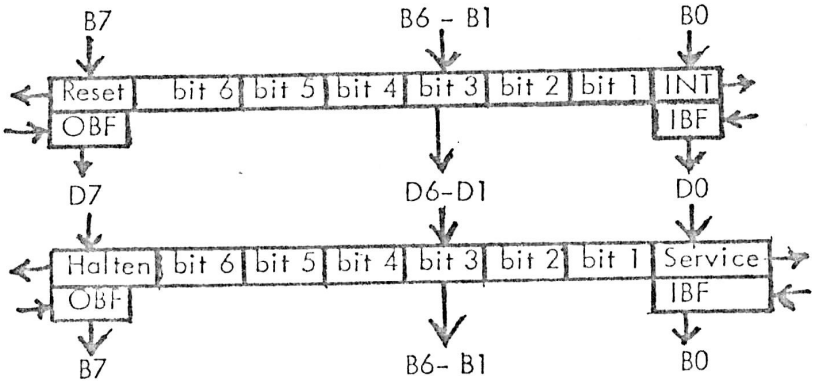
where: PSR = Processor Status Register
CCR = Calculator Control Register
IB = input buffer
OB = output buffer

* Resets input buffer full bit(IBF)
** Sets output buffer full bit(OBF)

3.3 The most and least significant bits of the PSR and CCR have different meanings depending on if the bits are written to or read from.

Bit	register	control	Function
least significant	CCR	RD	Input buffer full bit
		WR	INT. Routed through inverter to $\overline{\text{INT}}$ pin.
	PSR	RD	Input buffer full bit
		WR	Service. Requests 1LA8/1MB1 interrupt.
Most significant	CCR	RD	Output buffer full bit
		WR	Reset. Routed through inverter to $\overline{\text{Reset}}$ pin.
	PSR	RD	Output buffer full bit
		WR	Halten. Enables halt logic for 1LA8/1MB1.

The PSR and CCR can be visualized as follows:



where bits 6 - 1 can be used by software handshake functions.

3.4 The 1MB5 will respond to the following 8049 addresses. Only bits D7, D1 and D0 are decoded.

Address D7,D1,D0	Control	Function
000	WR	write to processor status register
	RD	read calculator control register
001	WR	write to input buffer and set input buffer full bit
	RD	read output buffer and reset output buffer full bit
010		set ADR2 pin high
011		set $\overline{\text{ADR3}}$ pin low

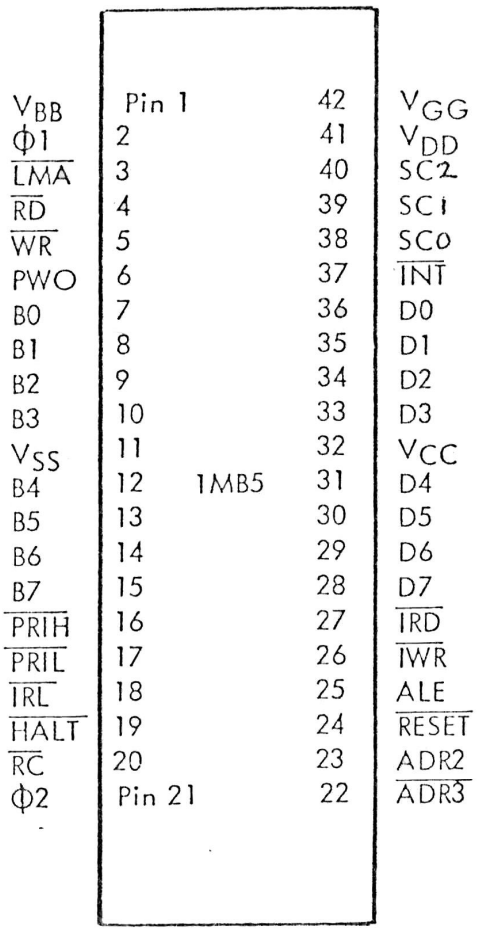

VBB Pin 1 42 VGG
Φ1 2 41 VDD
LMA 3 40 SC2
RD 4 39 SC1
WR 5 38 SC0
PWO 6 37 INT
B0 7 36 D0
B1 8 35 D1
B2 9 34 D2
B3 10 33 D3
VSS 11 32 VCC
B4 12 1MB5 31 D4
B5 13 30 D5
B6 14 29 D6
B7 15 28 D7
PRIH 16 27 IRD
PRIL 17 26 IWR
IRL 18 25 ALE
HALT 19 24 RESET
RC 20 23 ADR2
Φ2 Pin 21 22 ADR3

Fig. 3.1

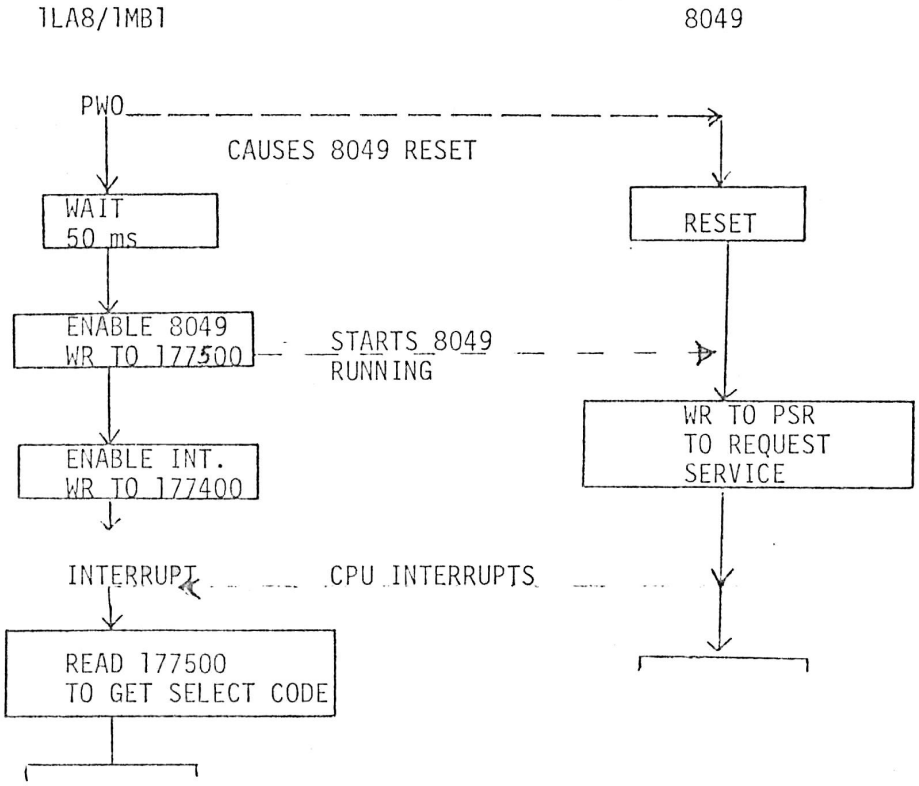
PIN DESCRIPTION

	Name	I/O	Pin#	Description
	B0-7	I/O	7-10 12-15	Three-state bidirectional data lines used to interface the 1MB5 to the 1MA8.
	$\overline{LMA}$	I/O	3	Load memory address. Active low to indicate the presence of an address on the bus. Driven high during a CPU halt.
	$\overline{RD}$	I/O	4	Read input. Active low to enable a read. Driven high while CPU is halted.
	$\overline{WR}$	I/O	5	Write input. Active low to enable a write. Driven high while CPU is halted.
	PWO	I	6	Power on. Resets chip to known state.
	$\phi 1, \phi 2$	I	2,21	Two non-overlapping clocks at 613 kHz.
	V_{GG}		42	+12 volt power supply
	V_{DD}		41	+6 volt power supply
	V_{CC}		32	+5 volt power supply
	V_{SS}		11	Circuit and supply ground
	V_{BB}		1	-5 volt power supply
	$\overline{PRIH}$	I	16	Priority input for interrupt logic.
	$\overline{PRIL}$	O	17	Priority output for interrupt logic.
	$\overline{IRL}$	O	18	Open drain interrupt request output.
	$\overline{Halt}$	O	19	Open drain halt request output.
	$\overline{RC}$	O	20	Open drain read control output.
*	D0-7	I/O	36-33 31-28	Three-state bidirectional data lines used to interface the 1MB5 to the Intel 8049.
*	$\overline{ALE}$	I	25	Address latch enable.
*	$\overline{IRD}$	I	27	Read input from 8049.
*	$\overline{IWR}$	I	26	Write input from 8049.
*	$\overline{INT}$	O	37	Interrupt output to 8049. Output is high at PWO.
*	$\overline{Reset}$	O	24	Hardware reset to 8049. Output is low at PWO.
*	ADR2	O	23	Address 2 detected output.
*	$\overline{ADR3}$	O	22	Address 3 detected output.
	SC0	I	38	Select code input. Grounded for a zero left open for a one.
	SC1	I	39	
	SC2	I	40	

Table 3.1

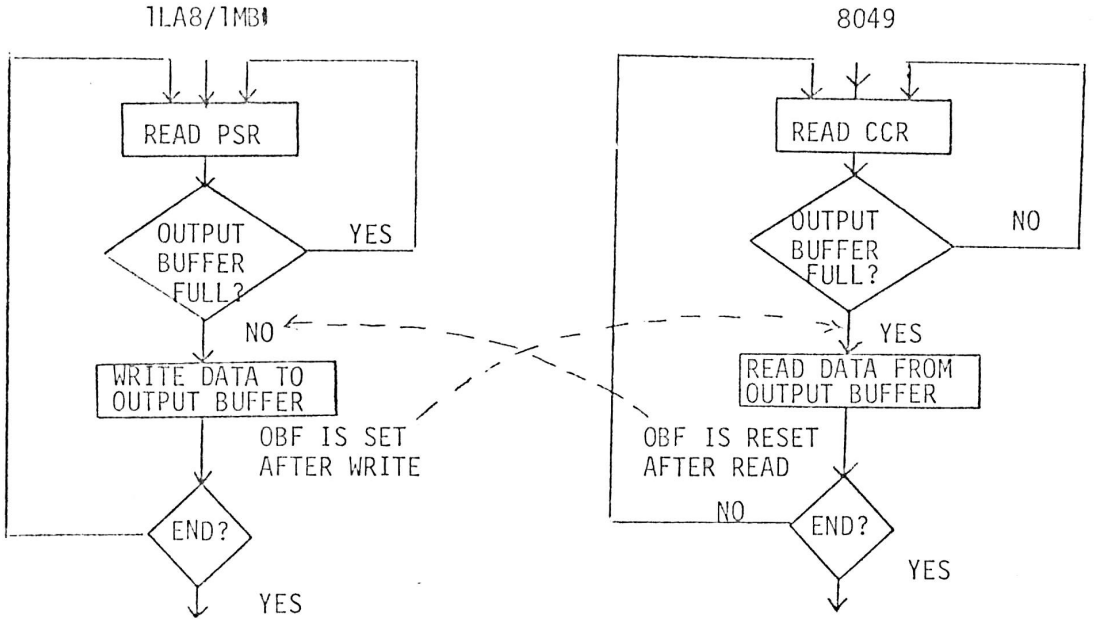
3.5 POWER-ON PROTOCOL

At power up time all 8049's are reset for 50 ms. When allowed to start running, each 8049 1MB5 chip pair causes the 1LA8/1MB1 to interrupt. This allows all select codes to be identified.

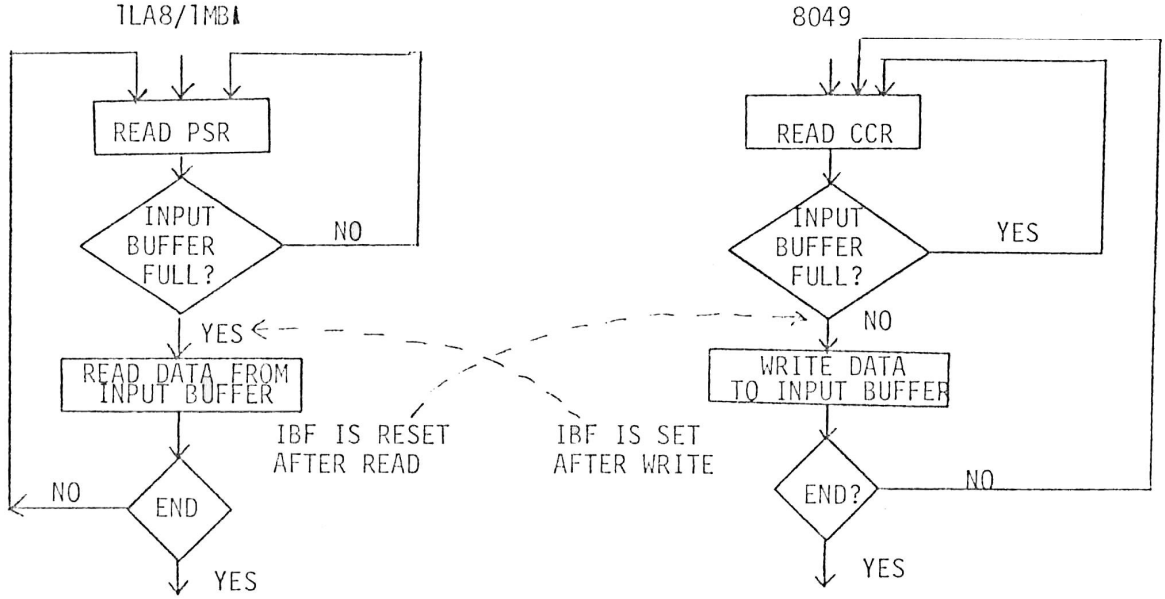


3.6 NORMAL HANDSHAKE MODE PROTOCOL

TO SEND DATA BYTE FROM 1LA8/1MB1 TO 8049



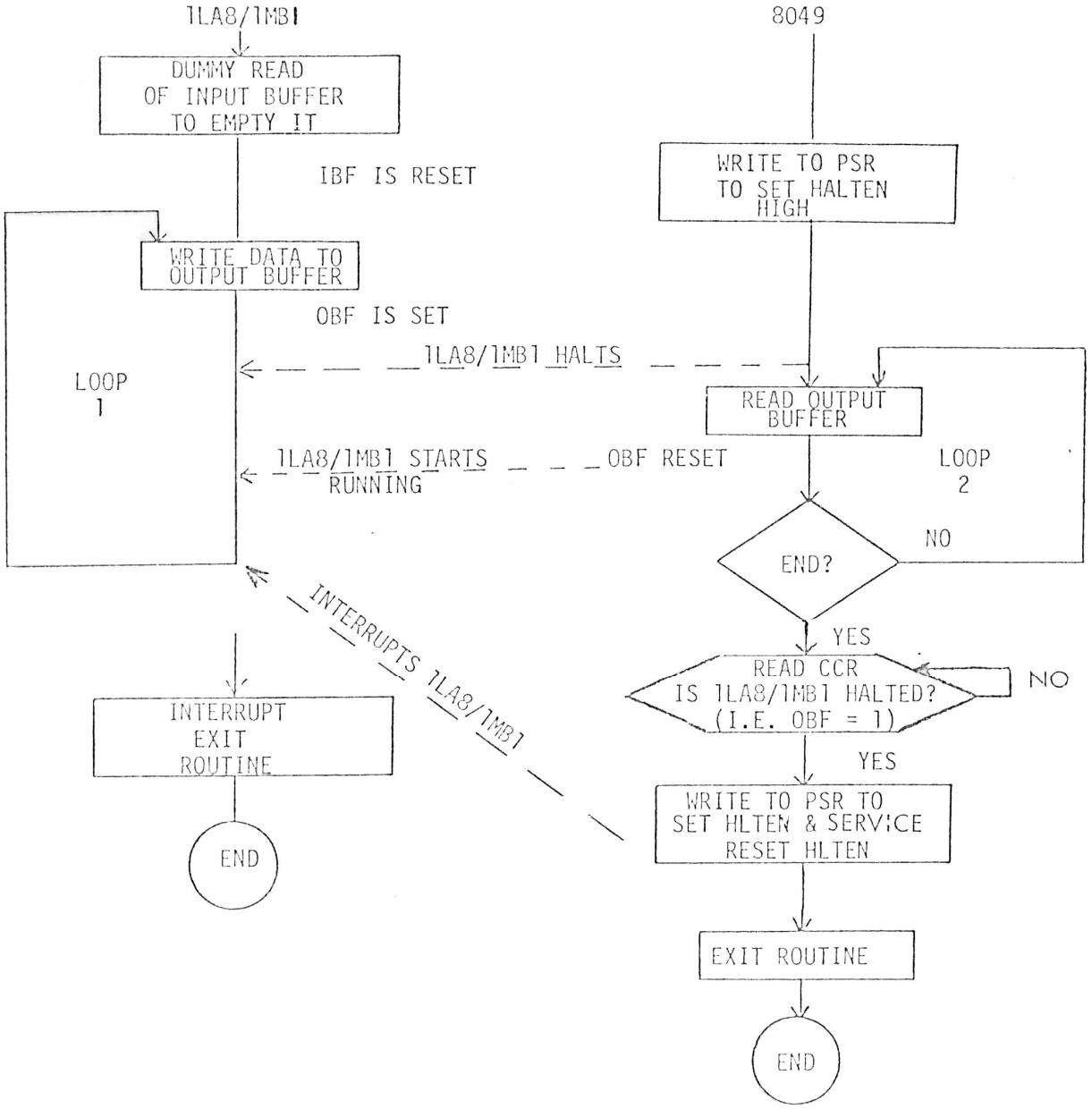
TO SEND DATA BYTE TO 1LA8/1MB1



	See	Sheet 1		MODEL	STK. NO 1MB5
				DETAILED SPECIFICATION - TRANSLATOR CHIP	
				BY T. KRAEMER	DATE 8-15-79
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 10 OF 10

3.7 BURST-OUT MODE PROTOCOL

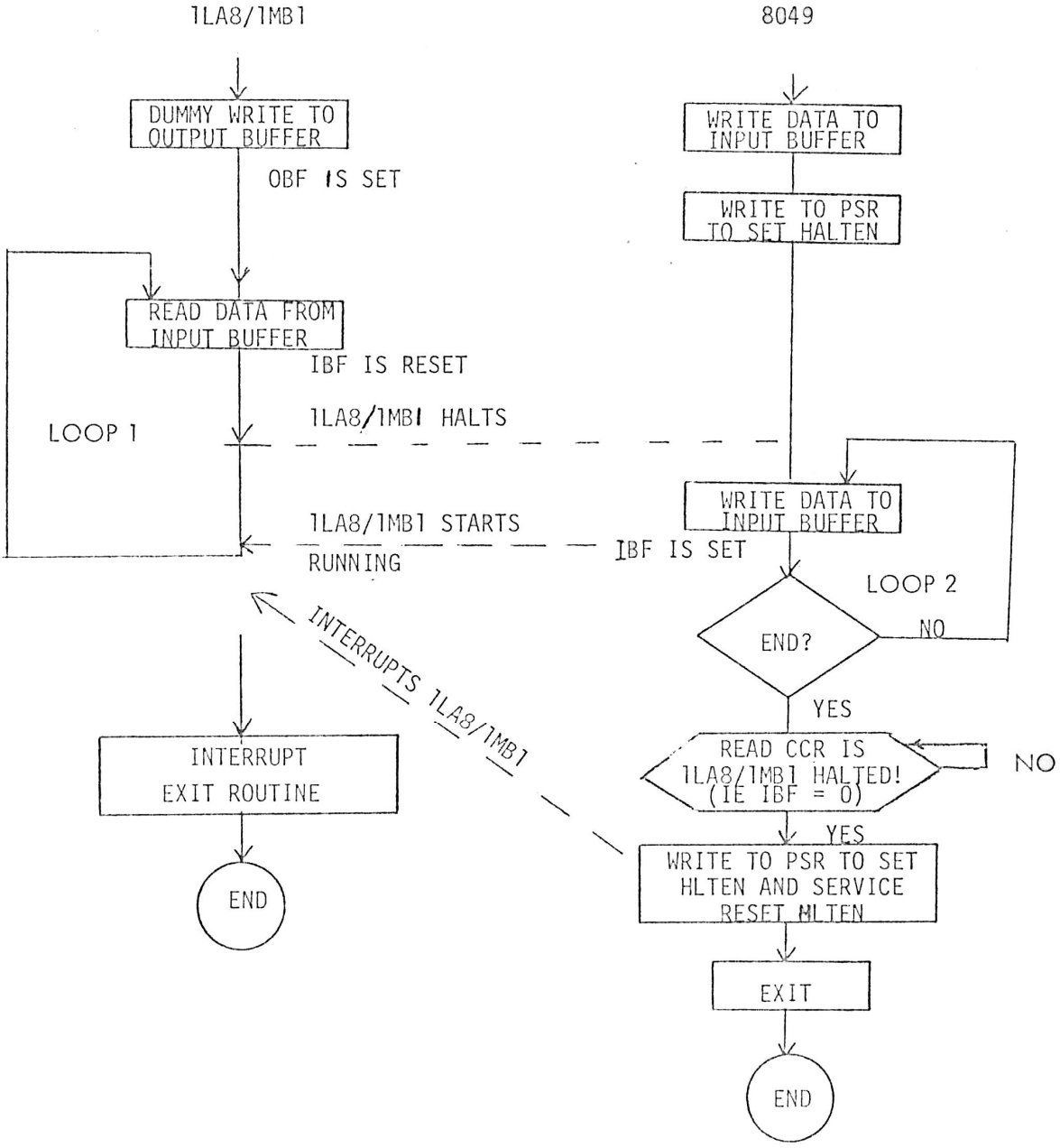
Burst out (interrupts enabled) in this mode it is assumed that Loop 1's execution time is less than Loop 2. Therefore, the 1LA8/1MB1 will halt and wait for Loop 2 to catch up.



	See	Sheet 1		MODEL	STK NO 1MB5
				DETAILED SPECIFICATION - TRANSLATOR CHIP	
				BY T. KRAEMER	DATE 8-15-79
				APPD	SHEET NO 11 OF 15
LTR	P.C. NO	APPROVED	DATE		

3.8 BURST-IN MODE PROTOCOL

Similar to burst-out protocol.



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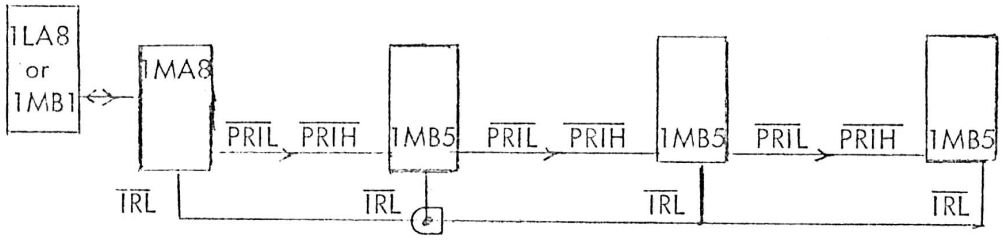
				DETAILED SPECIFICATION - TRANSLATOR CHIP	
				BY T. KRAEMER	DATE 8-15-79
LTR	P.C. NO	APPROVED	DATE	APPD	SHEET NO 12 OF 15

3.10 INTERRUPT PROTOCOL

For the 1MB5 to generate an interrupt request the following conditions are required:
1.) $\overline{PRIH} = 1$
2.) The service bit must go from a logic 0 to a logic 1. (As a result $\overline{PRIL}$, $\overline{IRL}$ go low)
3.) The interrupt logic must be enabledby a write to 177400 and 177500.

After an interrupt acknowledge is received (int ack = LMA·RD·WR = 1) the 1MB5 will drive the bus with its interrupt address vector $(020)_8$.

Hardware priorities are implemented with $\overline{PRIH}$, and $\overline{PRIL}$. The $\overline{IRL}$ output is wired anded with other interrupting devices.

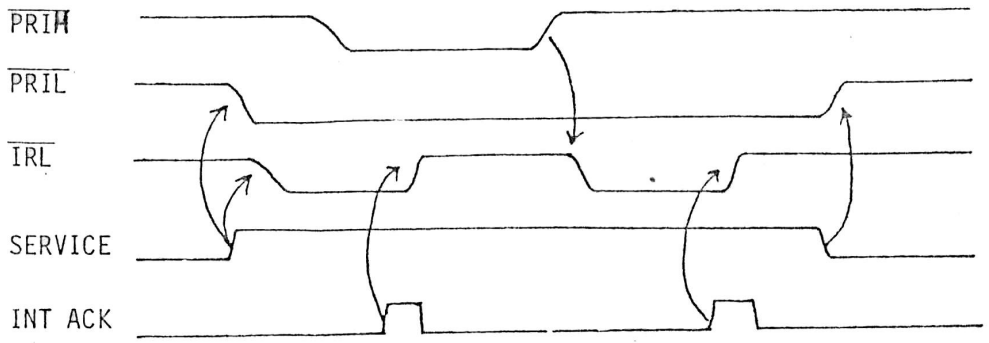


Three variations exist to handle multi-level interrupts:

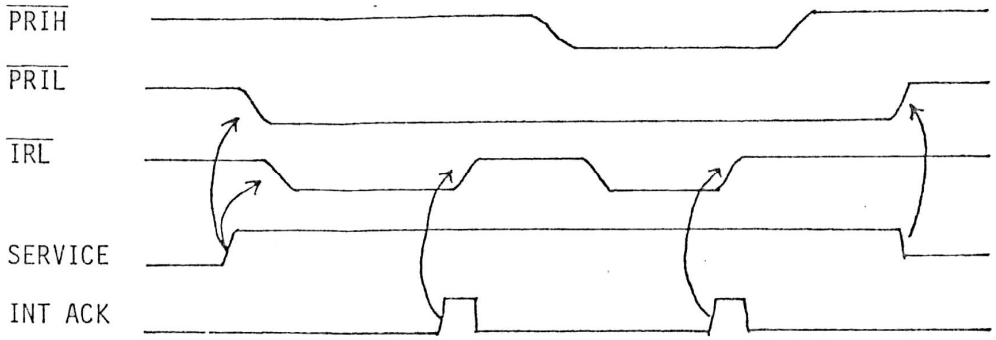
I. Lower priority device interrupts.
If $\overline{PRIH} = 1$ and my service bit is 0 and an interrupt acknowledge is received then the 1MB5 disables it s interrupts. The 1MB5 will remain disabled from interrupting until a write to 177500 is received.

II. Higher priority device interrupts before interrupt acknowledge is received.
If $\overline{PRIH}$ goes low before interrupt acknowledge is received then the 1MB5 chip will wait until $\overline{PRIH}$ goes high again and it will generate another interrupt request. This is shown in Fig. 3.2.

III. Interrupt acknowledge has been received and a higher priority device interrupts.
If $\overline{PRIH}$ goes low after an interrupt acknowledge has been received then the 1MB5 chip will wait until $\overline{PRIH}$ goes high again. This is also shown in Fig. 3.2.



$\overline{\text{PRIH}}$ GOES LOW BEFORE INTERRUPT ACKNOWLEDGE



$\overline{\text{PRIH}}$ GOES LOW AFTER INTERRUPT ACKNOWLEDGE

FIGURE 3.2

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Kyoto Ceramic 42 lead package KO-77227

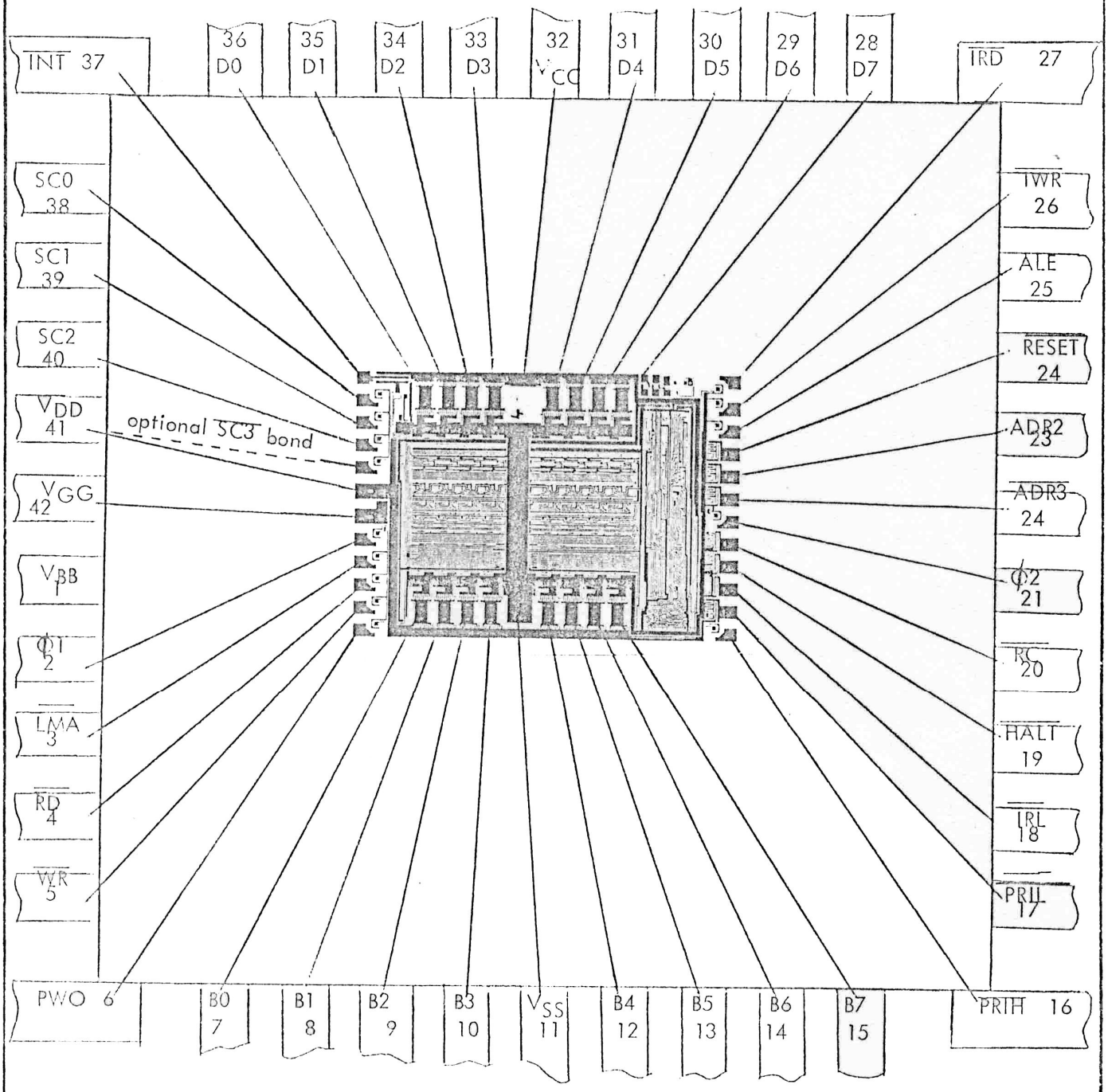

Fig. 3.3 Bonding Option .

	See	Sheet 1		MODEL	STK. NO. 1MB5
				DETAILED SPECIFICATION - TRANSLATOR CHIP	
				BY T. KRAEMER	DATE 8-15-79
LTR	P.C. NO	APPROVED	DATE	APPD	SHEET NO 15 OF 15